Not Entered

Preliminary Amendments to the claims

(Amendments under Article 34)

CLAIMS

1. A method of manufacturing a semiconductor device said method forming metal wirings of a predetermined pattern connected through a conduction path to a control electrode on an insulating layer formed on a substrate, said method comprising the steps of:

forming a metal film;

forming, on said metal film, a hard mask with a film thickness of at least 180 nm but not greater than 230 nm, said hard mask containing a silicon system inorganic insulating film, and said hard mask having said predetermined pattern; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said predetermined pattern;

wherein, in said step of forming said metal wiring, the amount of electric charge in said metal film is decreased to reduce the occurrence of the breakdown and deterioration, caused by said electric charge flowing into said control electrode, of said insulating layer.

2. A method of manufacturing a semiconductor device according to claim 1, wherein said hard mask is made of silicon oxide.

3. A method of manufacturing a semiconductor device according to claim 1, wherein said metal film is at least one of an Al film and an Al alloy film.

4. A method of manufacturing a semiconductor device according to claim 1, wherein said metal film is made of at least one of a tungsten film and a copper alloy film.

5. A method of manufacturing a semiconductor device according to claim 1, wherein a barrier metal film is provided.

6. A method of manufacturing a semiconductor device according to claim 5, further comprising the step of etching said barrier metal film by use of said hard mask.

7. A method of manufacturing a semiconductor device according to claim 1, wherein an antireflection film is provided between said metal film and said hard mask.

8. A method of manufacturing a semiconductor device according to claim 7, further comprising the step of etching said antireflection film by use of said hard mask.

9. A method of manufacturing a semiconductor device according to claim 1, wherein said etching gas contains Cl.

10. A method of manufacturing a semiconductor device having metal wirings of a predetermined pattern, said method comprising the steps of:

forming, on an insulating layer, a control electrode for a metal-insulator-semiconductor type device;

forming a metal film connected through a conduction path to said control electrode;

forming, on said metal film, a hard mask with a film thickness of at least 180 nm but not greater than 230 nm, said hard mask having said predetermined pattern and containing a silicon type inorganic insulating film; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said predetermined pattern.

11. A method of manufacturing a semiconductor device according to claim 10, further comprising the step of forming said insulating film prior to forming said control electrode on said insulating layer.

12. A method of manufacturing a semiconductor device according to claim 10, further comprising the step of forming a source and a drain for said metal-insulator-semiconductor type device.

13. A method of manufacturing a semiconductor device according to claim 10, wherein said hard mask is made of silicon oxide.

14. A method of manufacturing a semiconductor device according to claim 10, further comprising the steps of:

forming a barrier metal film prior to forming said metal film; and

etching said barrier metal film by use of said hard mask.

15. A method of manufacturing a semiconductor device according to claim 10, further comprising the steps of:

forming an antireflection film on said metal film prior to forming said hard mask on said metal film; and

etching said antireflection film by use of said hard mask.

16. A semiconductor device comprising:

a substrate;

a MIS type device having an electrode provided on an insulating film between said electrode and said substrate;

a metal wiring layer provided on said MIS type device by way of an interlayer insulating film, said metal wiring layer having a predetermined pattern; and

a hard mask, provided on said metal wiring layer, having

a predetermined pattern identical to that of said metal wiring layer;

wherein the film thickness of said hard mask is at least 180 nm but not greater than 230 nm; and

wherein said metal wiring layer is electrically connected to said electrode of said MIS type device.

17. A semiconductor device comprising:

a substrate;

a MIS type transistor having a source and a drain provided on the substrate; and a control electrode for controlling a current flowing between said source and drain, said control electrode being provided on an insulating film, said insulating film being provided between said control electrode and said substrate;

a metal wiring layer provided on said MIS type transistor by way of an interlayer insulating film, said metal wiring layer having a predetermined pattern; and

a hard mask, provided on said metal wiring layer, having a predetermined pattern identical to that of said metal wiring layer;

wherein the film thickness of said hard mask is at least 180 nm but not greater than 230 nm; and

wherein said metal wiring layer is electrically connected to said control electrode of said MIS type transistor.

16. A semiconductor device according to claim 17, wherein said MIS type field-effect transistor is a MOS type field-effect transistor.